				3				Page 1 of 1			
•	•	FORM	PTO-1449 N	16 3 0 2004 E	ATTY. DOCKET NO. APPLICATION NO. SP015.C16 (1397.028000G) 10/697,257 FIRST NAMED INVENTOR: NGUYEN et al.						
			70-14-0	ATEMENTA							
INFOR	MATION	N DISC	LOSURE	& TRADE	FILING DATE October 31, 2003		ART UNIT 2183				
	, ———	T====		U.S. P/	ATENT DOCUMENTS						
EXAMINER INITIAL		NUM	UMENT BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE			
INVIDAL.	AA8	1.00			TV SIVIL	102000	OOD-OLAGO	TILING DATE			
	AB8	ļ									
	ABO	ţ					-				
	AC8										
$\mathcal{L}(\Lambda)$	AD8	4,833	599	05/23/1989	Colwell et al.			 			
00,		<u> </u>			Colwell Ct al.						
W	AE8	4,974	,154	11/27/1990	Matsuo						
1/1	AF8	5,142	,634	08/25/1992	Fite et al.						
_ <u> </u>	AG8							•			
	AH8							,			
	AI8							<u> </u>			
	AJ8										
	AK8										
				FOREIGN	PATENT DOCUMENTS	s '		l			
EXAMINER		200	31.14.4F.1F	5475	0011117771						
NITIAL			CUMENT MBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION			
	1							Yes			
	AL7	HÉI	2-130635	05/18/1990	 			X Yes			
	AM7				712			No No			
	AN7					ļ		Yes			
		+	 					No Yes			
	A07			ļ	 			No			
	AP7					ļ		Yes No			
		,	OTHER (ncluding Auth	or, Title, Date, Pertine	nt Pages, et	c.)				
Ω	AR	<u>32</u>	Findlay, et al., "HARP: A VLIW RISC Processor", Proceeding of 5 th Annual European Computer Conference on Advanced Computer Technology, Reliable Systems and Applications, May 16, 1991, pp. 368-372.								
W	AS	<u>32</u>	Kuga et al., "DSNS (Dynamically-hazard-resolved, Statically-code-scheduled, Nonuniform Superscalar): Yet Another Superscalar Processor Architecture", Dept. of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan, pp. 14-29.								
0	АТ	<u>32</u>	Colwell et al., "A VLIW Architecture For A Trace Scheduling Compiler", Association For Computing Machinery (ACM), 1987, pp. 180-192.								
XAMINER	•		1			DAT	E COMSIDERED	1/1			
XAMINER: Initi	al if refere	ence coi	nsidered, what	her or not citation is	s in conformance with MPEP	609 Draw line	hrough offstigh if ha	in conformance			
nd not considere	d. Induc	е сору	of this form wi	n next communical	tion to Applicant.			comonnance			
			/				1.				

305006_1.DOC

SKGF Rev. 12/03/03

				LAF 18							
				DEC 2 2 2004	ATTY. DOCKET NO. SP015.C16 (1397.028000G)		Page 1 of 1 APPLICATION NO. 10/697,257				
		FORM	PTO-1449	DEC 5 5 2	FIRST NAMED INVENTOR: NGUYEN et al.						
INFORMATION DISCLOSURE ST				MEMENT NO.	FILING DATE		ART UNIT				
					October 31, 2003	1	2183				
EXAMINER INITIAL		DOC	UMENT BER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE			
	AA8					1					
	AB8										
	AC8										
1/4	AD8	4,833,599		05/23/1989	Colwell et al.						
n	AE8	4,974,154		11/27/1990	Matsuo						
4	AF8	5,142,634		08/25/1992	Fite et al.						
	AG8										
	AH8										
-	AI8										
	AJ8										
	AK8				-						
				FOREIGN	PATENT DOCUMENT	S	<u> </u>				
EXAMINER INITIAL		DOCUMENT NUMBER		DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION			
	AL7							Yes No			
W	AM7	HEI2-130635		05/18/1990	JP			X Yes			
	AN7			- "-				Yes No			
	A07							Yes No			
	AP7							Yes No			
			OTHER (Including Auth	or, Title, Date, Pertine	nt Pages, etc	.)				
\mathcal{M}	AR	<u>32</u>	Conference 368-372.	al., "HARP: A VLI" on Advanced Co	W RISC Processor", Proc Imputer Technology, Relia	eeding of 5 ⁿ An able Systems an	nual European C d Applications, N	Computer May 16, 1991, pp.			
N	/AS	<u>32</u>	Kuga et al., "DSNS (Dynamically-hazard-resolved, Statically-code-scheduled, Nonuniform Superscalar): Yet Another Superscalar Processor Architecture", Dept. of Information Systems, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan, pp. 14-29.								
N	AT	<u>32</u>	Colwell et a Machinery (II., "A VLIW Archit (ACM), 1987, pp.	ecture For A Trace Scheo 180-192.	duling Compiler"	, Association For	Computing			
XAMINER			MI.	an			CONSIDERED	11/10			
EXAMINER: Initia	al if refere	nce be	nsidered whet	her or not citation is	in conformance with MPEP	609. Draw line th	rough citation of no	in conformance			